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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/583,791	HE, JIANFEI	
	Examiner	Art Unit	
	KHALID ABDALLA	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :06/21/2006 and 08/02/2006 and 03/06/2007.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Field et al (US-PAT-NO: 6621828) in view of Diaz et al (US-PAT-NO:580921)

Regarding claim1 Field et al disclose an integrated cross-switching unit (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30 AND fig. 2), which is used for a Time

Division Multiplexing (TDM) system comprising a TDM line unit and a data service processing unit (Integrated access devices often combine synchronous and asynchronous transport and switch functionality to multiplex data, voice, and video traffic together onto a single network. Within an integrated access device, a time division multiplex (TDM) bus is typically used to transport voice and other synchronous traffic between the line cards and a switch core. An asynchronous transfer mode (ATM) bus is used to transport ATM traffic between the line cards and the switch core see co1:1 lines 41-50), comprising:

a bus identification module (The ATM line cards 40 perform header translation by

identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37);

a cross-connecting module (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30);

a mapping/de-mapping module (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look-up on the VPINCI, IP destination address and/or other suitable information and mapping it to one of 64K CID's see co1:16 lines 41-45);

an encapsulation/de-encapsulation module (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent encapsulation/de-encapsulation see co1:6 lines 38-46).

; and

a packet scheduling module (ATM adaption layer (AAL) cell traffic, and segmented packet traffic on a frame-based schedule see co1:6 lines 26-28 also see secheduller 356 of fig. 17) ; wherein

the bus identification module is adapted to identify a traffic source, to transmits traffic (The ATM line cards 40 perform header translation by identifying the coming virtual path

identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37). from the TDM line unit to the cross-connecting unit and to transmits packets from the data service processing unit to the packet scheduling module(ATM adaption layer (AAL) cell traffic, and segmented packet traffic on a frame-based schedule see co1:6 lines 26-28 also see secheduller 356 of fig. 17);

the cross-connecting module is adapted to schedule time slots of the traffic from the TDM line unit(The scheduler 356 manages outgoing slot allocation and incoming slot allocation. For outgoing slot allocation, the scheduler 356 specifies whether the multi\- purpose ATM switch 66 or the bus fuser 350 writes to a given outgoing slot see co1:19 lines 65-67 and clon:7 lines 1-2) ,

the mapping/de-mapping module is adapted to de-map the traffic (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look\- up on the VPINCI, IP destination address and/or other suitable information and mapping it to one of 64K CID's see co1:16 lines 41-45) from the cross-connecting module, and to map traffic from the encapsulation/de-encapsulation (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent encapsulation/de-encapsulation

see col: 6 lines 38-46) module;

the encapsulation/de-encapsulation module is adapted to de-encapsulate the traffic from the mapping/de-mapping module (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look\- up on the VPINCI, IP destination address and/or other suitable information and mapping it to one of 64K CID's see co1:16 lines 41-45), and to encapsulates the packets from the packet scheduling module; and

the packet scheduling module is adapted to schedule packets from the encapsulation/de-encapsulation module and/or the bus identification module (The ATM line cards 40 perform header translation by identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37) or to the TDM line unit via the encapsulation/de-encapsulation module, the mapping/de-mapping module and the cross-connecting unit in turn(The ATM line cards 40 perform header translation by identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37) although Field et al disclose (the scheduled packet and the encapsulation/de-encapsulation module, the mapping/de-mapping module) but he dose not explicitly disclose to transmit the scheduled packets to the data service processing unit via packet bus. Diaz et al from the same or similar field of endeavor teach to transmit the scheduled packets to the data service processing unit via packet bus (Data from a T1/E1 interface is placed onto the ingress bus in a VT format Each interface is provided

with an egress STS-1/TU-3 pointer processor and a VT mapper/demapper which performs the translation between T1/E1 and VT1.5/VT2 respectively see COLN:24 LINES 38-42). Thus it would have been obvious to one of ordinary skill in the art to implement the method of Diaz et al in the system of Field et al .The method of Field et al can be implemented on any type of method to transmit the scheduled packets to the data service processing unit via packet bus which is taught by Diaz et al with a motivation in order to provide flexible support various forms of telecommunications information services.

Regarding claim 2 Field et al discloses the integrated cross-switching unit (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30), wherein a plurality of physical channels are configured between the mapping/de-mapping module (In operation, DS-0 channels from a service interface are mapped into the TSB frame 100 in an arbitrary although fixed manner, with the TSI 64 of the fused TDM/ATM switch card 60 having the same mapping for switching the traffic to a destination card within the integrated access device 14 see co1:12 lines 35-39 and FIG.7) and the encapsulation/de-encapsulation module, and between the encapsulation/de-encapsulation module and the packet scheduling module (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in

order to map the packet flow into a cell flow and that therefore inherent encapsulation/de-encapsulation see col: 6 lines 38-46).

Regarding claim 3 Field et al discloses the integrated cross-switching unit according to claim 2, wherein the plurality of physical channels (switch card for a telecommunications node includes a shared memory operable to store traffic channels see co1:2 lines 9-10) are configured with different encapsulation protocols respectively(The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent different encapsulation/de-encapsulation protocols see co1:6 lines 38-46).

Regarding claim 4 ,Field et al discloses the integrated cross-switching unit (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30), wherein for the GFP frames from different physical channels, the encapsulation/de-encapsulation module finds CID field in the extended header of each GFP frame and directly forwards the data GFP frame with the CID field into the corresponding physical channel (A port value specifies the logical line port that traffic in the HSA slot 202 has originated from in the case of egress cells or is destined to in the case of ingress cells. For the CID field 240, the line card 40 replaces any protocol-specific header information such as VPINCI

with a unique CID value that is used by the switch core 44 to switch the cell see coln: 15 lines 46-53).

Regarding claim 6, Field et al discloses a traffic scheduling method (a scheduler 356 that coordinates the entire switched fuse operation see col: 19 lines 62-63) comprising the steps of:

A) a bus identification module identifying a traffic source (The ATM line cards 40 perform header translation by identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37). transmitting traffic from the TDM line unit to a cross-connecting module (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30) , and going to step B); and

B) the cross-connecting module scheduling the traffic from the TDM line unit, and going to step E); (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent encapsulation/de-encapsulation see co1:6 lines 38-46)

C) a mapping/de-mapping module de-mapping the traffic from the cross-connecting module and mapping traffic from an encapsulation/de-encapsulation module; (The ATM line cards 40 also perform ATM layer function such as processing operation,

administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent encapsulation/de-encapsulation see co1:6 lines 38-46)

D) an encapsulation/de-encapsulation module de-encapsulating the traffic from the mapping/de-mapping module and encapsulating packets from the packet scheduling module; (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent encapsulation/de-encapsulation see co1:6 lines 38-46).

and

E) the packet scheduling module scheduling packets from the encapsulation/de-encapsulation module and/or the bus identification module, and; transmitting scheduled packets to the data service processing unit via packet bus, or to the TDM line unit via the encapsulation/de-encapsulation module, the mapping/de-mapping module and the cross-connecting module in turn (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look\- up on the VPINCI, IP destination address and/or other suitable information and mapping it to one of 64K CID's see co1:16 lines 41-45).

Field et al discloses all the subject matter of the claimed invention with the exception of transmitting packets from a data service processing unit to a packet scheduling module via packet bus, and going to step E) . Diaz et al from the same or similar field of endeavor teach transmitting packets from a data service processing unit to a packet scheduling module via packet bus, and going to step E) (Data from a T1/E1 interface is placed onto the ingress bus in a VT format Each interface is provided with an egress STS-1/TU-3 pointer processor and a VT mapper/demapper which performs the translation between T1/E1 and VT1.5/VT2 respectively see COLN:24 LINES 38-42). Thus it would have been obvious to one of ordinary skill in the art to implement the method of Diaz et al in the system of Field et al .The method of Field et al can be implemented on any type of method transmitting packets from a data service processing unit to a packet scheduling module via packet bus, and going to step E) which is taught by Diaz et al with a motivation in order to provide flexible support various forms of telecommunications information services.

Regarding claim 7 ,Field et al discloses The method according to claim 6, wherein the identifying traffic source comprises (The ATM line cards 40 perform header translation by identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPI/VCI with a cell connection identifier (CID) see co1:6 lines 34-37): a slot number corresponding to the data service processing unit and unit type of the data service processing unit to a control unit via the data service processing unit (the controller 652 generates an address based on the line card 40 and HSA slot number of the cell for ingress ATM cells, the controller 652 access an ingress RAM 670

in the controller RAM 654 to determine a queue for storing the cell see col: 30 lines 62-66).

Field et al discloses all the subject matter of the claimed invention with the exception of identifying the type of a bus connected with the data service processing unit as a packet bus . Diaz et al from the same or similar field of endeavor teach identifying the type of a bus connected with the data service processing unit as a packet bus (Data from a T1/E1 interface is placed onto the ingress bus in a VT format Each interface is provided with an egress STS-1/TU-3 pointer processor and a VT mapper/demapper which performs the translation between T1/E1 and VT1.5/VT2 respectively see COLN:24 LINES 38-42). Thus it would have been obvious to one of ordinary skill in the art to implement the method of Diaz et al in the system of Field et al .The method of Field et al can be implemented on any type of method identifying the type of a bus connected with the data service processing unit as a packet bus which is taught by Diaz et al with a motivation in order to provide flexible support various forms of telecommunications information services.

Regarding claim 8 ,Field discloses The method according to claim 6,
further comprising:
the TDM line unit and the data service processing unit copying the traffic to a first integrated cross-switching unit and a second integrated cross-switching unit which have the same function and structure to implement the same scheduling (the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch

card. In this embodiment, the first switch slot includes both a low speed and high speed connector to connect the standard switch card to the low speed TDM bus and the high speed ATM bus while the second switch slot includes only a high speed connector to connect the high capacity switch card to the high speed ATM bus see co1:6 lines 63- 67 and co1:7 lines 1-8) ;

if the first integrated cross-switching unit and the second integrated cross-switching unit are both normal, the TDM line unit and the data service processing unit receiving the traffic from the first integrated cross-switching unit and the second integrated cross-switching unit, and selecting either of the traffic to implement a

processing (the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card. In this embodiment, the first switch slot includes both a low speed and high speed connector to connect the standard switch card to the low speed TDM bus and the high speed ATM bus while the second switch slot includes only a high speed connector to connect the high capacity switch card to the high speed ATM bus see co1:6 lines 63- 67 and co1:7 lines 1-8);

if either of the first integrated cross-switching unit and the second integrated cross-switching unit goes wrong (The protect set of switch cards 60 and 62 receives traffic in the protect mode from the TSB and HSA buses 70 and 72. If either of the active switch cards 60 or 62 fail, both of the cards are taken out of service and the protect set of switch cards is activated to perform necessary switching functionality see co1:10 lines 1-6), the faulted integrated cross-switching unit reporting to the control unit, and the

control unit instructing the TDM line unit and the data service processing unit to select the traffic of the normal integrated cross-switching unit .(The rate adjustable backplane 46 includes a set of switch slots 54 and a plurality of line slots 56. The set of switch slots 54 include one or more receptors for receiving one or more switch cards forming the switch core 44. In one embodiment, the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card see co1:6 lines 62-67 and co1:7 lines 1-7).

Regarding claim 9 ,Field et al discloses the method according to claim 6, further comprising:

the TDM line unit and the data service processing unit copying the traffic to the a first integrated cross-switching unit and the a second integrated cross-switching unit which have the same function and structure to implement the same scheduling (the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card. In this embodiment, the first switch slot includes both a low speed and high speed connector to connect the standard switch card to the low speed TDM bus and the high speed ATM bus while the second switch slot includes only a high speed connector to connect the high capacity switch card to the high speed ATM bus see co1:6 lines 63-67 and co1:7 lines 1-8)

the TDM line unit and the data service processing unit receiving the traffic from the first integrated cross-switching unit and the second integrated cross-switching unit,

determining whether the two traffic is normal, and selecting either of them traffic to implement a processing if the two are traffic is both normal (additionally, line card 40 to line card 40 processor communication can be achieved via processor generated cells directed to the loop-back to a different line card port 48. In this case, the OLB bit is set by the line card 40 but the port number attached to the cell is changed to that of the destination port 48 to allow the switch card 44 to switch the cell according to its normal port numberNPINCI/OAM look\- up processes to the desired line card port 40 with the egress OAM bit set see co1:15 lines 28-36); if either of the
traffic is abnormal, selecting the normal traffic (The rate adjustable backplane 46 includes a set of switch slots 54 and a plurality of line slots 56. The set of switch slots 54 include one or more receptors for receiving one or more switch cards forming the switch core 44. In one embodiment, the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card see co1:6 lines 62-67 and co1:7 lines 1-7) also (The protect set of switch cards 60 and 62 receives traffic in the protect mode from the TSB and HSA buses 70 and 72. If either of the active switch cards 60 or 62 fail, both of the cards are taken out of service and the protect set of switch cards is activated to perform necessary switching functionality see co1:10 lines 1-6).

Regarding claim 10 ,Field et al discloses The method according to claim 6, further comprising:
the TDM line unit and the data service processing unit allocating the traffic to a first

integrated cross-switching unit and a second integrated cross-switching unit which have the same function and structure to implement scheduling (the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card. In this embodiment, the first switch slot includes both a low speed and high speed connector to connect the standard switch card to the low speed TDM bus and the high speed ATM bus while the second switch slot includes only a high speed connector to connect the high capacity switch card to the high speed ATM bus see co1:6 lines 63-67 and co1:7 lines 1-8);

if the first integrated cross-switching unit and the second integrated cross-switching unit are both normal, the TDM line unit and the data service processing unit receiving the traffic from the first integrated cross-switching unit and the second integrated cross-switching unit to implement a processing (The rate adjustable backplane 46 includes a set of switch slots 54 and a plurality of line slots 56. The set of switch slots 54 include one or more receptors for receiving one or more switch cards forming the switch core 44. In one embodiment, the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card see co1:6 lines 62-67 and co1:7 lines 1-7) if either of the first integrated cross-switching unit and the second integrated cross-switching unit goes wrong, the faulted integrated cross-switching unit reporting to a control unit, and the control unit instructing the TDM line unit and the data service processing unit to switch the traffic allocated to the faulted integrated cross-

switching unit to the normal integrated cross-switching unit (The protect set of switch cards 60 and 62 receives traffic in the protect mode from the TSB and HSA buses 70 and 72. If either of the active switch cards 60 or 62 fail, both of the cards are taken out of service and the protect set of switch cards is activated to perform necessary switching functionality see co1:10 lines 1- 6).

Regarding claim 11 ,Field et al discloses The method according to claim 6, further comprising:

the TDM line unit and the data service processing unit allocating the service traffic to a first integrated cross-switching unit and a second integrated cross-switching unit which have the same function and structure to implement scheduling (the set of switch slots 54 include a first switch slot configured to receive a multiple format standard switch card and a second switch slot configured to receive an optional high capacity switch card. In this embodiment, the first switch slot includes both a low speed and high speed connector to connect the standard switch card to the low speed TDM bus and the high speed ATM bus while the second switch slot includes only a high speed connector to connect the high capacity switch card to the high speed ATM bus see co1:6 lines 63-67 and co1:7 lines 1-8);

the TDM line unit and the data service processing unit receiving the traffic from the first integrated cross-switching unit and the second integrated cross-switching unit and determining whether the traffic is normal (The protect set of switch cards 60 and 62 receives traffic in the protect mode from the TSB and HSA buses 70 and 72. If either of the active switch cards 60 or 62 fail, both of the cards are taken out of service and the

protect set of switch cards is activated to perform necessary switching functionality see co1:10 lines 1-6) if either of the traffic is abnormal, switch the traffic of the integrated cross-switching unit corresponding to the abnormal traffic to the normal integrated cross-switching unit (additionally, line card 40 to line card 40 processor communication can be achieved via processor generated cells directed to the loop-back to a different line card port 48. In this case, the OLB bit is set by the line card 40 but the port number attached to the cell is changed to that of the destination port 48 to allow the switch card 44 to switch the cell according to its normal port numberNPI/VCI/OAM look-up processes to the desired line card port 40 with the egress OAM bit set see col: 15 lines 28-36).

Regarding claim 12 ,Field et al discloses the method according to claim 9, wherein the traffic allocated to the first integrated cross-switching unit and the second integrated cross-switching unit has-priorities; when either of the integrated cross-switching units goes wrong (The DLP value identifies cell priority level for queuing purposes. In an exemplary embodiment, the DLP value ranges from 0-3, with a "0" value being the highest priority that therefore inherent high-priority service can substitute the low-priority service under processing see col: 14 lines 5-8) and needs traffic switching, the high-priority traffic substitutes the low-priority traffic under processing.(Referring to FIG. 10, CT byte 3, and bytes 5-8 are reserved. CT byte 4 concludes a 2 bit delay processing (DLP) field 222. The DLP value identifies cell priority level for queuing purposes. In an exemplary embodiment, the DLP value ranges from 0-3, with a "0" value being the highest priority see coln:14 lines 3-8)

Regarding claim 13 ,Field et al discloses The method according to claim 10, wherein the service allocated to the first integrated cross-switching unit and the second integrated cross-switching unit has priority; when either of the integrated cross-switching units goes wrong (The DLP value identifies cell priority level for queuing purposes. In an exemplary embodiment, the DLP value ranges from 0-3, with a "0" value being the highest priority that therefore inherent high-priority service can substitute the low-priority service under processing see col: 14 lines 5-8).and needs service switching, the high-priority service can substitute the low-priority service under processing .(Referring to FIG. 10, CT byte 3, and bytes 5-8 are reserved. CT byte 4 concludes a 2 bit delay processing (DLP) field 222. The DLP value identifies cell priority level for queuing purposes. In an exemplary embodiment, the DLP value ranges from 0-3, with a "0" value being the highest priority see coln:14 lines 3-8)

Regarding claim 14, Field et al discloses The integrated cross-switching unit (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30 AND fig. 2),

wherein the TDM line unit is a synchronous digital hierarchy or synchronous optical network line unit (synchronous digital hierarchy (SDH) traffic and other suitable types of traffic in which routing information is derived from the position of the traffic in a frame see co1:5 lines 62-65).

3. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Field et al (US-PAT-NO: 6621828) in view of Kumar et al (US 20020075854 A1).

Regarding claim 5 Field et al discloses an integrated cross-switching unit (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, see co1:6 lines 28-30), which is used for a TDM system including a TDM line unit and a data service processing unit (FIG. 1 illustrates a telecommunications system 10 in accordance with one embodiment of the present invention. The telecommunications system 10 transmits voice, data, video, other suitable types of information, and/or a combination of different types of information between source and destination points see col: 4 lines 51-57), comprising:

a bus identification module (The ATM line cards 40 perform header translation by identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37);

a high-order cross-connecting module (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, that therefore inherent both higher and lower order cross-connecting module see co1:6 lines 28-30);

a high-order mapping/de-mapping module (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look-up on the VPINCI, IP destination address

and/or other suitable information and mapping it to one of 64K CID's that therefore inherent both higher and lower order mapping/de-mapping module see co1:16 lines 41-45);

a high-order encapsulation/de-encapsulation module (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent both higher and lower order encapsulation/de-encapsulation see co1:6 lines 38-46)

a high-order packet scheduling module (ATM adaption layer (AAL) cell traffic, and segmented packet traffic on a frame-based schedule that therefore inherent both higher and lower order packet scheduling module see co1:6 lines 26-28);

a low-order cross-connecting module (the switch core 44 may also convert traffic between the TDM and ATM realms to establish cross connections between the line cards 40, that therefore inherent both higher and lower order cross-connecting module see co1:6 lines 28-30);

a low-order mapping/de-mapping module (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look-up on the VPINCI, IP destination address and/or other suitable information and mapping it to one of 64K CID's that therefore

inherent both higher and lower order mapping/de-mapping module see co1:16 lines 41-45);

a low-order encapsulation/de-encapsulation module (The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent both higher and lower order encapsulation/de-encapsulation see col: 6 lines 38-46); and

a low-order packet scheduling module (The ATM line cards 40 perform header translation by identifying the coming virtual path identifier (VPI)/virtual channel identifier (VCI) in cells and replacing the VPINCI with a cell connection identifier (CID) see co1:6 lines 34-37).the data service and/or TDM service from the TDM line unit to the high-order cross-connecting module, and transmits the data service from the data service processing unit to the high-order packet scheduling module (ATM adaption layer (AAL) cell traffic, and segmented packet traffic on a frame-based schedule that therefore inherent higher order packet scheduling module see co1:6 lines 26-28);

wherein

the bus identification module is adapted to identify a traffic source, to transmit traffic from the TDM line unit to the high-order cross-connecting module, and to transmits service packets from the data service processing unit to the high-order packet scheduling module (the switch core 44 may also convert traffic between the TDM and

ATM realms to establish cross connections between the line cards 40, that therefore inherent lower order cross-connecting module see co1:6 lines 28-30);

the high-order cross-connecting module is adapted to schedule the traffic as required for low-order processing to the low-order cross-connecting module, and to perform high-order scheduling on time slots of the traffic from the TDM line unit the low-order cross-connecting module is adapted to perform low-order scheduling on time slots of the traffic from the TDM line unit

the high-order and low-order mapping/de-mapping modules (the port and VPI fields of an incoming ATM cell are translated by the line card 40 to the unique CID value the line cards 40 generate the CID for each cell by performing a look-up on the VPINCI, IP destination address and/or other suitable information and mapping it to one of 64K CID's that therefore inherent higher order mapping/de-mapping module see co1:16 lines 41-45) are adapted to de-map the traffic from the high-order and low-order cross-connecting modules correspondingly, and to map traffic from the high-order and low-order encapsulation/de-encapsulation modules respectively;

the high-order and low-order encapsulation/de-encapsulation modules (The scheduler 356 manages outgoing slot allocation and incoming slot allocation. For outgoing slot allocation, the scheduler 356 specifies whether the multi-purpose ATM switch 66 or the bus fuser 350 writes to a given outgoing slot see co1:19 lines 65-67 and clon:7 lines 1-2) are adapted to de-encapsulate the traffic from the high-order and low-order mapping/de-mapping modules correspondingly, and to encapsulate the packets from the high-order and low-order packet scheduling modules respectively (The ATM line

cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent both higher and lower order encapsulation/de-encapsulation see col: 6 lines 38-46)
the high-order packet scheduling module is adapted to schedule packets from the high-order encapsulation/de-encapsulation module and/or the bus identification module and via the high-order encapsulation/de-encapsulation module (ATM adaption layer (AAL) cell traffic, and segmented packet traffic on a frame-based schedule that therefore inherent both higher and lower order packet scheduling module see co1:6 lines 26-28) , the high-order mapping/de-mapping unit; and the high-order cross-connecting module in turn (the switch and line cards are synchronized to this 125 microsecond frame pulse which in turn is derived from the systems clock see co1:32 lines 24-26) that therefore inherent both higher and lower order cross-connecting module) ,the low-order packet scheduling module receives the data
the low-order packet scheduling module is adapted to schedule packets from the low-order encapsulation/de-encapsulation module and scheduling; to transmit the scheduled packets to the TDM line unit via the low-order encapsulation/de-encapsulation module(The ATM line cards 40 also perform ATM layer function such as processing operation, administration, and management (OAM) cells and perform monitoring functions. Packet based line cards 40 segment and resemble (SAR) packets into

generic ATM cells. Ethernet line cards 40 examine source address (SA) and destination address (DA) of the ethernet packets in order to map the packet flow into a cell flow and that therefore inherent lower order encapsulation/de- encapsulation see co1:6 lines 38-46), the low-order mapping/de-mapping module and the low-order cross-connecting module in turn (the switch and line cards are synchronized to this 125 microsecond frame pulse which in turn is derived from the systems clock see co1:32 lines 24-26). Field et al does not disclose to transmit the scheduled packets to the data service processing unit via packet bus or to the TDM line unit. Kumar et al from the same or similar field of endeavor teach (Media abstraction unit 850 includes a transmit path and a receive path. The transmit path of media abstraction unit 850 converts optical signal from optical transceiver 820 into an electrical data stream and reframes the data stream into a stream of electrical data frames that has a size particularly suited for wireless transmission ; The receive path of media abstraction unit 850 reframes electrical data frames from RF wireless unit 840 or free-space optics unit 830 into TDM frames such as SONET/SDH/PDH frames and then converts the data stream into an optical signal. The optical signal is sent to optical transceiver 820 and then to physical layer interface 810. see[0053] . Thus it would have been obvious to one of ordinary skill in the art to implement the method of Kumar et al in the system of Field et al .The method of Field et al can be implemented on any type of method to transmits the scheduled packets to the data service processing unit via packet bus or to the TDM line unit which is taught by Kumar et al with a motivation in order to provide a hybrid network to carry synchronous and asynchronous traffic over symmetric and asymmetric links.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(US 20030179717 A1) , (Hobbs et al) disclose , methods and apparatus for controlling multi-layer communication networks.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHALID ABDALLA whose telephone number is (571)270-7526. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton can be reached on 571-272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. A./
Examiner, Art Unit 2419

/DANG T TON/
Supervisory Patent Examiner, Art Unit 2419/D. T. T./
Supervisory Patent Examiner, Art Unit 2419